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1.	Your reference	**P035005GB: HRG**
2.	Patent application number *(The Patent Office will fill in this part)*	30 JUL 2003 0317854.8 31JUL03 E826615-1 D00019 P01/7700 0.00-0317854.8
3.	Full name, address and postcode of the or of each applicant *(underline all surnames)*	**ELEMENT SIX LIMITED ISLE OF MAN FREEPORT BALLASALLA ISLE OF MAN IM99 6AQ**
	08479958001 Patents ADP number *(if you know it)*	
	If the applicant is a corporate body, give the country/state of its incorporation	**UNITED KINGDOM**
4.	Title of the invention	**METHOD OF MANUFACTURING DIAMOND SUBSTRATES**
5.	Name of your agent *(if you have one)*	**Carpmaels & Ransford**
	"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	**43 Bloomsbury Square London WC1A 2RA**
	Patents ADP number *(if you know it)*	**83001**
6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number	Country Priority application number *(if you know it)* Date of filing *(day / month / year)*
7.	If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application	Number of earlier application Date of filing *(day / month / year)*
8.	Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if: a) any applicant named in part 3 is not an inventor, or b) there is an inventor who is not named as an applicant, or c) any named applicant is a corporate body See note (d))*	Yes

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Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	1
Request for preliminary examination and search *(Patents Form 9/77)*	
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Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature: Carpmaels & Ransford
Carpmaels & Ransford

Date: **30th July 2003**

12. Name and daytime telephone number of person to contact in the United Kingdom

DR. HUGH GOODFELLOW 020-7242 8692

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BACKGROUND OF THE INVENTION

THIS invention relates to a method of manufacturing single crystal diamond substrates for use in device applications, and to diamond wafers for use in such a method.

Diamond offers a range of unique properties, including optical transmission, thermal conductivity, stiffness, wear resistance and electronic properties. Whilst many of the mechanical properties of diamond can be realised in more than one type of diamond, other properties are very sensitive to the type of diamond used. For example, for the best electronic and other properties, CVD single crystal diamond is important, often outperforming polycrystalline CVD diamond, HPHT diamond and natural diamond.

There are many applications where the workable area or surface of the final diamond product is very small. In such applications it is often difficult to achieve economies of scale or to provide practical methods of processing the single crystal diamond substrates into the desired devices. Thus, for example, the manufacture of electronic devices on the surfaces of small individual diamond substrates is problematic. Conventional lithographic techniques and existing lithography equipment are not suited to realising some of the complex electronic structures envisaged for such single crystal diamond substrates.

SUMMARY OF THE INVENTION

According to the present invention, a method of producing single crystal diamond substrates, in particular for device applications and more particularly for electronic applications, includes the steps of providing a plurality of single crystal diamond plates, each diamond plate having a backing surface and an opposite surface, hereinafter the fabrication surface, arranging the diamond plates adjacent one another in a substantially planar orientation with their respective backing surfaces exposed, bonding a backing layer to, or forming a backing layer on, the exposed backing surfaces of the diamond plates so as to fix the diamond plates to the backing layer, and processing as required the fabrication surfaces of the respective fixed diamond plates to produce respective single crystal diamond substrates. The single crystal diamond substrates are suitable for subsequent forming of device structures on said fabrication surfaces.

The backing layer is preferably a polycrystalline diamond layer. The polycrystalline diamond layer may be bonded to the plurality of crystal diamond plates by any appropriate means such as, for example, gluing or brazing. Particularly preferred, however, is that the polycrystalline diamond layer is grown onto the plurality of single crystal diamond plates, thereby forming a direct diamond to diamond bonding between layer and plates.

The processing of the fabrication surfaces will typically be to provide for electronic or other device features on the fabrication surfaces.

The invention extends to a diamond wafer for use in a method of manufacturing single crystal diamond substrates, the diamond wafer comprising a plurality of single crystal diamond plates fixed to a polycrystalline diamond backing layer in a substantially planar arrangement such that a major surface of the respective fixed diamond plates is exposed for optional further processing. The invention further extends to such

wafers used for subsequent processing of the single crystal diamond substrates into device structures using wafer scale techniques.

The invention also extends to a method of manufacturing such a diamond wafer, and to the subsequent separation of such a wafer into the individual single crystal diamond plates and individual devices, for example by cleavage of the polycrystalline diamond layer between the single crystal diamond substrates, and where required by cleavage of the single crystal diamond substrates along appropriately formed grooves or by other means.

The diamond wafer is preferably dimensioned so as to be suitable for use in conventional lithography techniques using existing lithography equipment.

DESCRIPTION OF PREFERRED EMBODIMENTS

The invention is directed to providing a tiled array of diamond plates which is suitable for wafer scale processing, for example, in the manufacture of electronic or other device structures on the diamond plates.

In order to be suitable for wafer scale processing, the diamond plates are preferably single crystal diamond plates. These single crystal diamond plates are preferably either CVD diamond having an accessible upper surface or alternatively present an accessible upper surface coated with a layer of CVD diamond.

The accessible surface of each plate, referred to as the "fabrication surface", is required to fall within a defined tolerance of a single conceptual plane, such that the fabrication surface of each plate within a wafer may be further processed by wafer scale techniques such as those described later. Thus, for instance, where photolithographical techniques are to be applied with a single plane of optical focus, the tolerance of the fabrication surfaces to the conceptual plane should be less than about 100 μm, preferably less

than about 25 µm, more preferably less than about 10 µm, even more preferably less than about 5 µm, and most preferably less than about 3 µm. Where mechanical processing techniques are to be applied to the respective fabrication surfaces, for instance, it is preferable that the fabrication surfaces fall within a defined tolerance of a single conceptual plane which is less than about 5 µm, preferably less than about 2 µm, more preferably less than about 1 µm, even more preferably less than about 0.5 µm, and most preferably less than about 0.2 µm.

The single crystal diamond plates or tiles are preferably arranged in an array such that the fabrication surface intended for use on each diamond plate is in an arrangement regular in the sense that it repeats from wafer to wafer, such that jigs for constructing the array and lithography masks or other wafer processing equipment are equally valid for each wafer. A preferred embodiment is where the regularity of the arrangement extends to the arrangement on a single wafer, such that the position of each plate can be described in terms of a regular two dimensional lattice, in a manner akin to atoms in a material lattice. In principle more than one plate can be associated with each lattice point, and each plate associated with a particular lattice point can be of a different geometry, but a preferred embodiment is the case when each single crystal plate is the same shape, and a further preferred embodiment is where there is only one single crystal diamond substrate plate associated with each lattice point.

One preferred embodiment is where the single crystal diamond plates are arranged to butt together in a well aligned array, or more preferably to be spaced apart by a small predetermined spacing. The small predetermined spacing is sufficient to avoid contact damage during mounting or thermal cycling, but not so large as to substantially reduce the total packing density on the backing layer. This spacing also avoids the problem of errors in one plate affecting the positioning of those in direct contact with it. Another preferred embodiment is where in addition the plates are all rectangular in form.

Those skilled in the art will understand that the existence of small defects in the geometry of individual plates, or in the positioning of individual plates in the array, do not invalidate the general concept of the regular array provided that such defects do not substantially degrade the yield obtainable in the final wafer scale processing.

The array of single crystal diamond plates or tiles is bonded to a backing layer, in particular a polycrystalline diamond layer, which provides matched thermal expansion and good thermal heatsinking during the processing thereof. The bond between the backing layer and the individual tiles can be provided in any appropriate manner such as gluing or brazing. However, in order to assist in the function of the diamond wafer, it should exhibit one or more of a high thermal conductivity, stability under high process temperature, for example up to 1100°C, and high mechanical strength to enable wafer scale mechanical processing. Brazing is acceptable for processing temperatures up to about 1100°C, and provides relatively good thermal conductivity and mechanical strength. However, it is preferred that a layer of polycrystalline diamond is grown onto the back surface of the array of single crystal diamond plates, which forms direct diamond to diamond bonding. The main advantages of this are that the thermal expansion match of the joint between the array of single crystals and their supporting layer is perfect, that there are no other materials present that could cause contamination to subsequent processes, and that the dielectric match between the backing or support layer and the array of single crystal diamond plates is the same.

It is preferred to use a set of single crystal diamond plates which are similar in size and shape to assist in mounting them into an array. However the required tolerances are much less than would be the case for a set of plates intended to butt together in a continuous array that is used for overgrowing a single diamond crystal without discernible boundaries on top. Likewise, aligning a series of non-contacting plates is easier than ensuring precise alignment and uniform regular contact between an array of contacting tiles. Furthermore, in the present invention, an error with one

tile position, shape or orientation affects only that tile, and does not affect the other tiles in the diamond wafer.

It is envisaged that the application of the diamond wafer may often benefit from the plates all presenting a similar crystallographic orientation within set limits. In order to achieve this, it is generally only necessary to prepare a single edge and/or a single major face of each of the plates with the necessary precision with respect to the crystal orientation of the plate. In the case of an edge this would be placed in contact with an alignment feature during the process of bonding the plates into an array. In the case of a major face, this aligned face, which would become the fabrication surface, would be placed against a reference plane during the process of bonding the plates and any non uniformity in the rear surfaces will be taken up by the bonding process.

The bonding of the array of single crystal diamond plates together with a polycrystalline diamond layer is preferred, as it provides excellent thermal expansion matching between the mounting and the individual plates, ensures maximum thermal conductivity, has a very high temperature stability enabling much higher temperature processes to be used on the plates, and has similar chemical inertness to the single crystal diamond plates so that aggressive chemistries can be used. In addition, following device fabrication onto the surfaces of the individual diamond plates making up the wafer, the device can be simply removed from the wafer by snapping through the polycrystalline diamond layer between the single crystal diamond plates.

For the purposes of this specification, the term 'device structures' referring to the structures fabricated onto the surface of the single crystal diamond substrates, refers to any heterogeneous or non-planar structure fabricated into or onto the surface of the single crystal diamond substrate in order to provide or modify the functionality as an electric device, electronic device, optical or mechanical device of which in final application the diamond forms an integral part. By way of non-limiting examples the following may be

considered: implanted doping for heater tracks, grooves provided for mechanical or thermal isolation, or for fibre positioning, such as may be used with laser diode arrays, simple or complex electronic devices, from a simple pi junction with contact metallisation, to multi-layer, multi-material, and/or multi-contact devices, optical elements such as micro lenses, micro mirrors for electro-optic or opto-electronic applications, and mechanical constructions such as beams, suspended masses etc. such as may be used in electromechanical devices such as accelerometers, pressure sensors etc.

The processing steps to produce device structures generally fall into two categories, those which are wafer scale in a simultaneous sense, and those which are wafer scale in a sequential sense.

Examples of wafer scale processes in a simultaneous sense include providing one or more metal layers combined with lithographic techniques and, for example, wet etching or dry plasma etching, to construct electrical contacts to the diamond. Other examples include further diamond coatings, such as doped diamond, to provide contact means or active elements of a device, or uniformly distributed ion implantation processes, and non-diamond coatings such as other semiconductor materials which may provide functional elements in the final devices.

Examples of sequential wafer scale processing include ion implantation using a scanning beam to write device features, where the ion implanter can be pre-programmed to automatically process the entire array of single crystal plates on an individual wafer in a sequential fashion. Similar examples are laser processing, to cut tracks in overlayers or into the diamond itself, and ion beam milling for the fabrication of small detail in devices.

Depending on the relative size of the single crystal diamond substrates and the desired device, there may be one or more devices fabricated into each single crystal diamond substrate. Where more than one device is so

formed, one of the wafer scale processes may be the provision of grooves such as those cut by laser into the single crystal substrates to provide means for separation of the devices subsequently, for example by cleavage along said grooves.

A further variant of the invention is where the single crystal plates bonded together by a polycrystalline diamond backing layer, are used as groups of plates in a further stage of processing or in the final application, still bonded together by said backing layer. These groups may include any number of the single crystal plates from more than one to the complete assembly of plates formed as the original wafer. In this variant of the invention, the processing of the single crystal plates once in the wafer form is optional, and may include steps such as providing uniform optical polish on one or even both major faces of the plates. In order to retain the strength of the plate assembly and yet enable the rear faces to be polished, the plates may be more widely separated to enable bonding to occur in between the plates rather than across the rear faces, for example so that during the synthesis of the polycrystalline diamond backing layer the wider spaced plates enable growth species to move into the gaps between the plates and form a polycrystalline diamond layer in this location. It may be advantageous to use means such as a backing layer to avoid the growth of the polycrystalline diamond layer onto the rear major face of the plates in this application. Final applications making use of such assemblies of plates include specialist heat sinks, complex sensor and electrical or electro-optic device applications, and multi-window optical applications.

The invention will now be illustrated by way of the following non-limiting example:

Example 1

A set of HPHT single crystal plates were prepared to the following criteria:

a) all the plates were selected from material showing no gross defects or strongly strained regions;

b) all <100> edged plates with no missing corners reducing the <100> edge length by > 15%;

c) all <100> edges between 3.8 and 4.0 mm;

d) all exposed major facets (the fabrication surface) within 2° of the {100};

e) all plates with their opposing major faces parallel to within 3°, and an overall thickness of 0.6 mm +/- 0.02 mm;

f) all plates with one reference edge aligned to the <100> direction to better than 3°; and

g) the fabrication surface finished to an Ra of < 10 nm and prepared in a manner suitable for subsequent electronic use.

The reverse surfaces of the single crystal plates that formed the array were lapped to a surface finish of >20nm to improve bonding to the subsequent polycrystalline diamond layer.

These single crystal plates were then placed into a prepared alignment mount which caused the individual plates to be closely packed but separated by a small 0.3 mm gap in a well aligned array. The lapped surfaces were placed uppermost. The mount was then placed into a CVD diamond reaction chamber and polycrystalline CVD diamond was formed onto the lapped surface of the array. Although in this example the polycrystalline diamond layer was 350 μm thick, the thickness of the polycrystalline layer can range from 1 or 2 μm through to several mm, if so desired.

Once the array was joined together by the polycrystalline diamond layer it was far more robust and could be handled as a single wafer, no longer requiring the mount to hold the individual crystals together.

The polycrystalline layer can be lapped or polished if required and the array of single crystal surfaces can also be further polished if so required by the subsequent processing steps.

The diamond wafer so produced is suitable for the further processing of the fabrication surfaces to produce single crystal diamond substrates suitable for electronic devices to be applied thereto.